Application Note 62

TMC22x5y Revision F Silicon Update

Revision F functional anomalies

1. Black level clamp problem with noisy input signals
2. PAL burst lock loop problem
3. Luma error [YESG] register bit problem
4. Mixed sync data can overflow when video inputs are over-blanked

The four outstanding functional anomalies are:

Black level clamp problem with noisy input sources

Systems containing low frequency white noise can produce lsb changes in the internal digital clamp level. A possible workaround is described in TMC22x5y_APPS4. Please note that when implementing this workaround, the SIMPLE selection controlled by the YMUX[1:0] and CMUX[1:0] register bits will select the VIDEOB data input. Also in PAL the luma signal on the first and last lines of active video is set to the value on the VIDEOB input. A second option on the workaround for PAL, is to program MSIP[1:0] = 0x during the active video lines and MSIP[1:0] = 1x during the vertical blanking period, remembering to include the first and last active video lines of each. field

PAL burst lock loop problem

To overcome this problem simply strobe the SET pin whenever the input is changed, a temporary loss of sync is detected, or just on a regular basis during the vertical sync interval. The ‘color kill’ operation becomes unstable when implementing this workaround because the SET function also resets the color kill circuit.

Luma error [YESG] register bit problem

If the luma error signal is doubled by setting the YESG register bit HIGH, the error signal overflows and does not clip as described in the data sheet. There is no work around for this problem.

Mixed sync overflow

The mixed sync data overflows if large positive luma signals are processed during the mixed blanking period, i.e. outside the AV period for active video lines. This mixed sync data is only used if the syncs are selected to be on the decoded outputs and the mixed sync gain, SG[9:0] is greater than zero. This problem can be resolved by simply under-blanking the input video, for example by setting AV[9:0] = 722 for inputs at a 13.5MHz data rate.

Register bit changes and/or clarification

a) register 44h bit 7 - ***MONO*** - LOW when color kill is active (i.e. when no burst is detected).

b) register 44h bits [6:0] ***FPERR[6:0]*** represents the top 7 bits of the modulo 2 pi phase error.

c) register 1Eh bit 0 - ***SYSPH[0]*** - inverts the V axis phase. For normal operation set this bit HIGH

d) register 16h bits [1:0] - ***MSIP[1:0]*** - the internal offset has been changed with relation to this signal. A 0H offset produces a delay of the F & V signals through the decoder equal to the delay through the comb filter. The 1H offset produces these signals one line earlier, because the reference is assumed to be one line later.

e) register 47h bits [7:0] - ***REVID*** - the rev E silicon revision number is 05h and the rev F silicon revision number is 06h.

f) register 0Ah bits [4:3] - ***MSEN[1:0]*** - should be set to 10 to pass super black signals even on D1 or other component signal outputs.